REMARKS

The enclosed is responsive to the Examiner's Office Action mailed on June 14, 2005. At the time the Examiner mailed the Office Action claims 1-28 were pending, and claims 11-17 were allowed. Applicant has made no amendments to the claims. The Applicant respectfully requests reconsideration of the present application and the allowance of all claims now presented.

Claim Rejections

35 U.S.C. 102(e) Rejections

The Examiner rejected claims 1-3, 5-9, 18, 19, 21, and 23-27 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Application Publication 2004/0043592 A1 by Goodwin et al. (hereinafter "Goodwin").

With respect to independent claim 1, Applicant teaches and claims: "A method comprising: forming a logic gate stack in a logic region on a substrate; forming a flash memory gate stack in a flash region on the substrate; depositing a hardmask layer over the logic gate stack and over the flash memory gate stack; patterning the hardmask in the logic region so that areas of hardmask remain where logic gates are desired; patterning the flash gate stack in the flash region to form flash memory gates; and etching the logic gate stack using the remaining hardmask as a mask to form logic gates." Applicant teaches the formation of flash memory gates from a flash memory gate stack and logic memory gates from a logic memory gate stack.

With respect to independent claim 18, Applicant teaches and claims: "An apparatus comprising: a substrate, the substrate having a logic region and a flash region; a logic gate stack formed on the substrate in the logic region, the logic gate stack having a top surface; regions of anti-reflective coating (ARC) formed on the top surface of the logic gate stack, the regions of ARC covering the areas of the logic gate stack where logic gates are to be formed; a plurality of flash memory gates formed on the substrate, the flash memory gates having a top surface; and a layer of resist, wherein the resist covers at least the top surface of the logic gate stack, the regions of ARC formed on top of the logic gate stack, and the top surface of the flash memory gates." Applicant teaches "a logic gate stack where logic gates are to be formed."

With respect to independent claim 24, Applicant teaches and claims: "A method comprising: forming a logic gate stack in a logic region on a substrate; forming a flash memory gate stack in a flash region on the substrate; depositing a hardmask layer over the logic gate stack and over the flash memory gate stack; patterning the hardmask in the logic region so that areas of hardmask remain where logic gates are desired; patterning the flash gate stack in the flash region and etching away the hardmask layer and a portion of the flash memory gate stack in the flash region to form a partial flash memory gate; and etching the logic gate stack and the remainder of the flash memory gate stack using the remaining hardmask as a mask to form logic gates and flash memory gates." Applicant teaches the formation of flash memory gates from a flash memory gate stack and logic memory gates from a logic memory gate stack.

Goodwin describes a method for forming a gate contact in a semiconductor device (page 1, paragraph 0001). The method taught by Goodwin is used after the gate of the semiconductor device (and/or the gate of the memory device) has already been formed. Etching of a gate stack to form gates as taught and claimed by Applicant is not taught by Goodwin.

For example, figures 2-6 illustrate how Goodwin forms a gate contact. Figure 2 illustrates a transistor device (100) which has already been formed (page 2, paragraph 0021). The transistor device includes a gate formed from gate dielectric 104 and two conductive layers 106 and 108 (page 2, paragraph 0022). The gate stack used by Goodwin has already been etched to form the gate of a device. Goodwin does not teach the process of etching the gate stack; Goodwin merely teaches that a device gate has been formed. Moreover, before Goodwin begins the formation of gate contacts, an insulated cap layer (110) is formed over the gate of the device. Goodwin does not teach formation of flash and logic gates from a gate stack, as taught by Applicant. Goodwin teaches formation of flash and logic gate contacts after the gates of the devices have been formed.

Similarly, figures 7-12 of Goodwin illustrate an embodiment having multiple transistors. Again, Goodwin begins in figure 7 with four completed transistors: memory devices (230a, 230b) and logic devices (240, 250). Note that the device gates for the transistors are already formed. See, for example, paragraph 0040: "four transistors are shown"; paragraph 0043: "transistors 230, 240, and 250 having been formed as discussed above"; paragraph 0044: "planarizing layer ... is formed over the device (including transistors 230, 240, and 250)"; and paragraph 0045: "the exposed portions of the nitride cap layer are removed from transistor 250". Goodwin

does not teach how the device gates are etched from gate stacks; Goodwin teaches only how to form gate contacts after the transistor gates have already been formed from a gate stack.

Goodwin does not teach the formation of gates from gate stacks. Goodwin does not teach etching or patterning a flash memory gate stack to form flash memory gates. Furthermore, Goodwin does not teach etching or patterning a logic gate stack to form logic gates. Therefore, Applicant respectfully submits that Goodwin does not anticipate all elements of independent claims 1, 18, and 24.

Claims 2-3, and 5-9 are dependent upon claim 1. Claims 19 and 21 are dependent upon claim 18. Claims 25-27 are dependent upon claim 24. Thus, for at least the same reasons advanced above with respect to independent claims 1, 18, and 24, Applicant respectfully submits that Goodwin does not anticipate all elements of dependent claims 2-3, 5-9, 19, 21, and 25-27.

With respect to independent claim 23, Applicant teaches and claims: "A method comprising: forming a first stack in a first region on a substrate and a second stack in a second region on the substrate, wherein the second stack is thicker than the first stack; depositing a hardmask layer over the first stack and the second stack; patterning the first region to remove portions of hardmask in the first region; patterning the second region to remove portions of the hardmask in the second region and portions of the second stack to form the desired geometries of the second stack; and removing portions of the first stack using the remaining portions of hardmask as a mask to form the desired geometries of the first stack." Two stacks of differing heights are formed, and a hardmask layer is deposited over the first stack and the second, thicker stack.

Goodwin does not teach forming a hardmask layer over a first stack and a second, thicker stack. Goodwin forms devices (Figs. 7 and 8, references 230, 240, 250) having a cap layer (208). Each device stack of Goodwin has the same height (see Fig. 7 & Fig. 8). An ARC layer (218) is formed around the devices, and a resist layer (220) is formed over the devices. After the resist is patterned, exposed portions of the cap layer (208) are removed from device 250, thus forming stacks of different heights. This is the opposite of what is done by the Applicant. The applicant first forms two stacks of different heights, then forms a hardmask over the stacks having different heights. Therefore, Applicant respectfully submits that Goodwin does not anticipate all elements of independent claim 23.

Applicant, accordingly, respectfully requests withdrawal of the rejections of claims 1-3, 5-9, 18, 19, 21, and 23-27 under 35 U.S.C. § 102(e) as being anticipated by Goodwin.

35 U.S.C. 103(a) Rejections

The Examiner rejected claims 4 and 20 under 35 U.S.C. 103(a) as being unpatentable over Goodwin in view of applicant's admitted prior art. The Examiner rejected claims 10, 22, and 28 under 35 U.S.C. 103(a) as being unpatentable over Goodwin.

Claims 4 and 10 are dependent upon independent claim 1. Claims 20 and 22 are dependent upon independent claim 18. Claim 28 is dependent upon independent claim 24. Thus, for at least the reasons advanced above with respect to independent claims 1, 18, and 24, Applicant respectfully submits that Goodwin does not render these dependent claims obvious.

Applicant, accordingly, respectfully requests withdrawal of the rejections of

claims 4, 10, 20, 22, and 28 under 35 U.S.C. § 103(a) as being unpatentable over Goodwin.

Allowable Subject Matter

Applicant has noted, with appreciation, that the Examiner has allowed claims 11-17 over the prior art of record.

CONCLUSION

Applicant respectfully submits that the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Michael A. Bernadicou at (408) 720-8300.

Pursuant to 37 C.F.R. 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully Submitted,

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